IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) A process for manufacturing an integrated circuit package comprising:

(a) forming a substrate having a first dielectric layer, a conductive layer having a first region insulated from a second region and located above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity wherein the first and second regions are exposed within the cavity; and

(b) interconnecting a first lead of an integrated circuit to the exposed first region and interconnecting a second lead of the integrated circuit to the exposed second region.

(2) Please amend Claim 7 as follows:

7. (Amended) A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) forming a first dielectric layer on a substrate;

(b) forming a conductive layer having a first region insulated from a second region, above the first dielectric layer;

(c) forming a second dielectric layer above the conductive layer; and

(d) forming a cavity in the second dielectric layer to expose the first and second regions of the conductive layer and coupling a first lead of the integrated circuit chip to the exposed first region and coupling a second lead of the integrated circuit to the exposed second region.

(3) Please amend Claim 12 as follows:

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12. (Amended) The method recited in Claim 7, further comprising coupling the integrated circuit chip to the substrate.

(4) Please amend Claim 13 as follows:

13. (Amended) A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) forming a first dielectric layer on a substrate;

(b) forming a conductive layer having a first region insulated from a second region, above the first dielectric layer;

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(c) forming a second dielectric layer above the conductive layer;

(d) forming a second conductive layer above the second dielectric layer; and

(e) forming a cavity in a first region of the second dielectric layer to expose the first and second regions of the first conductive layer and coupling a first lead of the integrated circuit chip to the exposed first region and a second lead of the integrated circuit chip to the exposed second region.

(5) Please amend Claim 16 as follows:

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16. (Amended) The method recited in Claim 13, further comprising coupling the integrated circuit chip to the substrate.

(6) Please cancel Claim 17 without prejudice or disclaimer.